A REVIEW OF LOW POWERAND AREA EFFICIENT FSM BASED LFSR FOR LOGIC BIST

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ABSTRACT

Built in Self Test circuits enable an integrated circuit to test itself. Built in Self Test reduces test and maintenance costs for an integrated circuit by eliminating the need for expensive test equipment. Built in Self Test also allows an integrated circuit to test at its normal operating speed which is very important for detecting timing faults. Despite all of these advantages Built in Self Test has seen limited use in industry because of area and performance overhead and increased design time. This paper presents automated techniques for implementing BIST in a way that minimizes area and performance overhead. This approach allows applying at-speed test patterns and eliminates the need for an external tester. Proper design of the test pattern generator contributes to reduction in the power consumption of the CUT and the overall power consumption of the BIST circuitry. We have proposed FSM based LFSR which generate maximum correlation among the patterns and targeted on c432, c1908 and c3540 benchmark circuits to validate test power, achieved significant improved in power up to 15% compared to conventional test generator and also achieved optimal area overhead,designed using Verilog HDL and implemented using Xilinx 14.3 and Cadence tool.

KEYWORDS

Logic BIST, Switching activity, Low power design, SIC BS LFSR& Fault coverage

1. INTRODUCTION

Testing of digital VLSI circuits entails many challenges as a consequence of rapid growth of semiconductor manufacturing technology and the unprecedented levels of design complexity. These challenges include keeping the average and peak power dissipation and test application time within acceptable limits. In complex VLSI circuits need to be decrease power dissipation because power dissipation during testing mode almost double compare to normal mode of operation [25]. Another challenging aspect is area overhead [5] of the circuits. For these problems need to design very efficient test pattern generator, that generate test patterns with minimum switching activity and also take less area without effecting other parameter s in circuit.

The previous works that have been done in the area of low power testing, especially the techniques that involved reducing transitions or toggles to reduce switching activity during the test. The section summarizes the work done for controlling power dissipation during testing circuits with BIST circuitry Ahmed N.Awad and Abdulla if S.AbhuIssa [3] presented the four different LFSR's technique to reduce the transitions between the test patterns for a Memory BIST. Girard [7] [8][9][10] proposed survey paper on low testing of VLSI circuits and also presented a method to reduce internal switching activity in circuits by decreasing the transition density at the inputs through test vector ordering. In [4] proposed A Novel BIST Scheme for Low

Power Testingmethod using SIC and modified LFSR that reduced test power.A.S.AbuIssa and S.F. Quigley [12] presented the modified LFSR that reduces the number of transitions at the input of the circuit under test by 25% using the bit swapping technique. Wang and Gupta [2] [13] presented a new BIST TPG design, called low-transition random TPG (LT-RTPG) that comprised an LFSR, a k-input AND gate, and a T flip-flop. The [1] [29] used concept of LT-LFSR and also focused on area overhead. The primary goals of this work are to develop an efficient test generation method for digital logic circuits to obtained high fault coverage and compare different LFSR scheme in terms of different parameters. Another part of this work is to develop a LFSR that has less number of transitionactivities in test patterns.

2. CIRCUIT UNDER TEST

The International Symposium for Circuits and Systems (ISCAS) has designed certain circuits called as the benchmark circuits that are extensively used in Design for Testability. The benchmark circuits when used in the BIST architecture as the Circuit under Test (CUT) help to clearly analyze the efficiency of a Test Pattern Generator used in testing. In proposed paper the ISCAS-85 Benchmark circuit C 432 a 27-channel interrupt controller with 36 primary inputs 7 primary outputs number of gates 160 and equivalent fault sets size are 524 similarly we have chosen more complex circuit with larger configurations with C1908 a 16-bit single error correcting and double error detecting (SEC/DED) circuit with some byte error detection capability and C3540 a 8 bit ALU with binary and BCD arithmetic, and logic and shift operations is used as CUT. The fault model used in design is stuck at fault model, s_a_0 means logic line permanently got short circuited with respect to ground (GND) and s_a_1 means logic line permanently got short circuited with respect to supply (Vcc)

Table 1. Configuration of Benchmark circuits

Benchmark circuit	**Primary Inputs**	**Primary Outputs**	**Number of gates**	**Equivalent fault set size**	**Fault Type**
C432 27-channel interrupt controller	36	7	160	524	{s_a_0 s_a_1}
C1908 16-bit SEC/DED circuit	33	25	880	1879	{s_a_0 s_a_1}
C3540 8-bit ALU	50	22	1669	3428	{s_a_0 s_a_1}

Table 1 showsdifferent benchmark circuits in terms of number of gates which includes AND,OR,XOR,NOT ,NAND and NOR gates and equivalent fault set size which includes stuck at 0 and 1.

3. GENERATION OF TEST VECTORS

3.1. Test Vector Generation using LFSR

A series of D-ffs with external exclusive-OR is called as standard LFSR [11]. The circuit representation of standard LFSR, as the name suggests, is basically a shift register having D flip-flops where the output of the last flip-flop provides feedback to the input of the first flip-flop. If there are n flip-flops$x_0, x_1, \ldots . x_{n-1}$,then the LFSR is called n -stage LFSR. The feedback is basically a linear XOR function of the outputs of the flip-flops. Output of any flip-flop may or may not participate in the XOR function; if output of any flip-flop X_i say, provides input to the XOR function then corresponding tap point h_i;(Figure 2) is 1. Similarly, if output of flip-

flop X_i does not provide input to the XOR function then corresponding tap point h_i is 0. In the circuit representation ifh_i =0, then there is no XOR gate in the feedback network corresponding to the output of the flip-flop X_i; otherwise, the XOR gate is included. Now, we give an example of a standard LFSR and illustrate the pattern generated the register and also shown an example of a standard LFSR.

This LFSR can also be described by the characteristic polynomial and matrix of LFSR also shown

$$f(x) = 1 + h_1 x + h_2 x^2 + \cdots + h_{n-2}\, x^{n-2} + h_{n-1}\, x^{n-1} + x^n$$

$$\begin{bmatrix} X_0(t+1) \\ X_1(t+1) \\ X_2(t+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} X_0(t) \\ X_1(t) \\ X_2(t) \end{bmatrix}$$

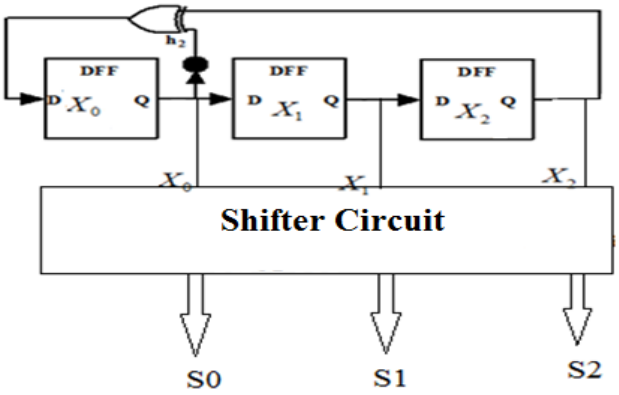

Figure 1: Standard LFSR with Shifter Circuit

It may be noted that output of flip-flop X_2 provides feedback to the XOR network, while flip-flop X_1does not; so $h_1 = 0$ and $h_2 = 1$. The characteristic polynomial of the LFSR is $f(x) = 1+x^2+x^3$.If the initial values of the flip-flops are $X_0=0$, $X_1=0$, $X_2=0$, then the sequence of patters is as follows: $f(x) = 1+x^2+x^3$

Table 2.Pattern generator using Shifter Circuit

X_0 X_1 X_2	S_0 S_1 S_2
1 0 0	1 0 0
1 1 0	0 1 0
1 1 1	0 0 1
0 1 1	1 0 1
1 0 1	1 0 1
0 1 0	1 1 0
0 0 1	0 1 1
1 0 0	1 0 0
1 1 0	0 1 0
1 1 1	0 0 1
0 1 1	1 0 1
0 0 1	0 1 1

So the LFSR generates 12 patterns (excluding all 0s) after which a pattern is repeated. It may be noted that this LFSR generates all patterns (except all 0s) which are generated by a 3 bit counter, however the area of the LFSR is much lower compared to a counter. In a real time scenario, the

number of inputs of a CUT is of the order of hundreds. So LFSR has minimal area compared to counters.

3.2. Statistics Report

The table 3 shows the synthesis report of standard LFSRused in top module, RTL compiler used to extract various parameters.

Table 3: Synthesis report of LFSR

Parameters	Total Power (mW)	Dynamic Power(mW)	Leakage Power(nW)	Area (cells)	Gates
Standard LFSR	0.11	0.10	0.28	5980	587

3.3 Test Vector Generation using FSM based LFSR

The proposed TPG structure combines two methods of test pattern generation called Random Injection (RI) and Bipartite LFSR. Briefly, the RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. The Bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns.

Figure 4 shows proposed in [1] , called LT LFSR used LFSR with RI and Bipartite LFSR, the random injector circuit taps the present state (T^i pattern) and the next state (T^{i1} pattern) of LFSR, signals en1 and en2 select half of the LFSR to generate random patterns, as shown in Figure 4 and 5.

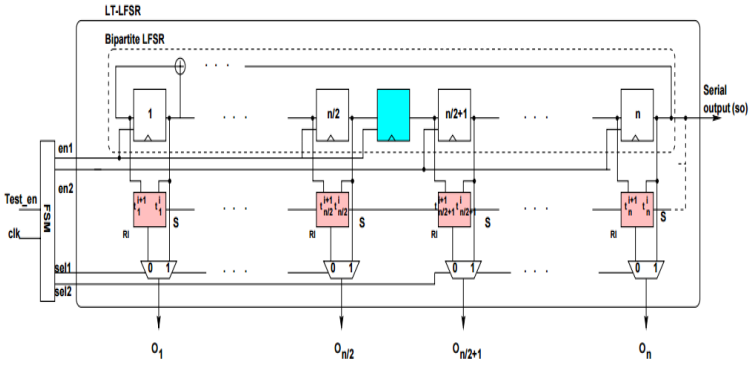

Figure 3. Low Transition LFSR(LT-LFSR)

3.3.1 Random Injection Methodology

To preserve the randomness of patterns, instead of Bipartite strategy, we randomly inject a value in bit positions, where $t_j^i \neq t_j^{i+1}$. Briefly

$$t_j^{i1} = \begin{cases} t_j^i if t_j^i = t_j^{i+1} \\ R if t_j^i \neq t_j^{i+1} \end{cases}$$

Figure 5 shows this symbolically, the shaded cells show those bit positions where $t_j^i \neq t_j^{i+1}$,we insert a random bit (shown as R inT^{i1}) if the corresponding bits in T^i and T^{i+1} are different. Note

that, since such bits are uniformly distributed and we also replace them with another random value, the overall randomness remains unchanged, that is, H_{max}= n. The maximum bit transition can no longer be guaranteed, although the expected number of transitions (mean value in the normal distribution) will be n/2.

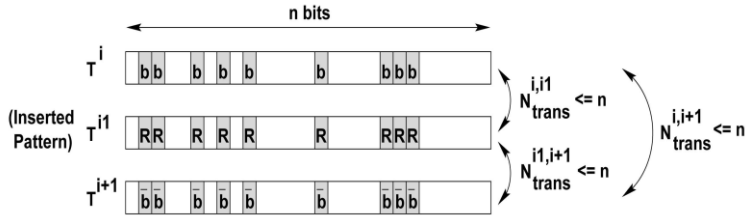

Figure 4: An example for RI

The below figure 6 shows the RI unit that generates intermediate patterns. R is a random bit which can come from one of the outputs of a random pattern generator i.e LFSR itself.

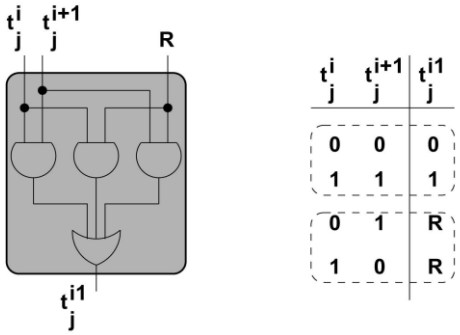

Figure 5: Random Injection (RI) circuit

4. IMPLEMENTATION OF PROPOSED TECHNIQUE

4.1. Implementing FSM based LFSR

We combine two proposed techniques of pattern generation (RI and Bipartite LFSR) for low-power BIST. The new LFSR generates three intermediate patterns (T^{i1}, T^{i2} , and T^{i3}) between T^{i} andT^{i+1}. We embed these two techniques into a bit-sliced LFSR architecture to create FSM based LFSR, which provides more power reduction compared to having only one of the Random Injection and Bipartite LFSR techniques in an LFSR. However, due to the high randomness of the inserted patterns, many of the intermediate patterns can do as well as patterns generated by an LFSR in terms of fault detection.

4.1.2. Algorithm for FSM based LFSR

Finite-state machine (FSM) controls the pattern generation process as follows:

Step 1. en1en2 = 10, sel1sel2 = 11. The first half of LFSR is active and the second half is in idle mode. Selecting sel1sel2 = 11, both halves of LFSR are sent to the outputs ($O_1$to O_n). In this case, T^{i} is generated.

Step 2. en1en2 = 00, sel1sel2 = 10. Both halves of LFSR are in idle mode. The first half of LFSR is sent to the outputs ($O_1$to$O_{\frac{n}{2}}$), but the RI injector circuit outputs are sent to the outputs ($O_{\frac{n}{2}+1} toO_n$). T^{i1}Is generated.

Step 3. en1en2 = 01, sel1sel2 = 11. The second half of LFSR works and the first half of LFSR is in idle mode. Both halves are transferred to the outputs ($O_1$to O_n) and T^{i2} is generated.

Step 4. en1en2 = 00, sel1sel2 = 01. Both halves of LFSR are in idle mode. From the first half, the injector outputs are sent to the outputs of LT-LFSR (O_1 to $O_{\frac{n}{2}}$) and the second half sends the exact bits in LFSR to the outputs ($O_{\frac{n}{2}+1} toO_n$) to generate T^{i3} .

Step 5. The process continues by going through Step 1 to generateT^{i+1}.

4.2. Synthesis Report of FSM based LFSR

The table below shows the synthesis report of FSM based LFSR when used in top module to extract various parameters. The Power consumption during testing, total power, Dynamic power are given in mW and Static power is given in nW, Area is given in number of cells and the total number of gates used.

Table 4: Synthesis of FSM based LFSR

Parameters	**Total Power (mW)**	**Dynamic Power(mW)**	**Leakage Power(nW)**	**Area (cells)**	**Gates**
FSM based LFSR	0.13	0.12	0.18	4370	487

4.3. Implementing Modified FSM based LFSR

We combine two proposed techniques of pattern generation (BSC and Ring Counter) for low-power BIST. We embed these two techniques into a bit-sliced LFSR architecture to create modified LFSR, which provides more power reduction compared to having only one of the Bit Selector Circuit and Ring Counter techniques in an LFSR.

4.3.1. Algorithm for Modified FSM based LFSR

Finite-state machine (FSM) controls the pattern generation process as follows:

Step 1: $s1s0$ = 11, the generated new test pattern is sent to CUT directly, if it has less vertical switching transitions.

Step 2: $s1s0$ = 00, LSB of test pattern is filled with random bits and MSB of present test pattern is frozen.

Step 3: $s1s0$ = 10, MSB of present test pattern is frozen and LSB is replaced by the new test pattern bits.

Step 4: $s1s0$ = 11, MSB is replaced by new test pattern and LSB is kept as it is.

Step 5: The process continues going through Step 1.

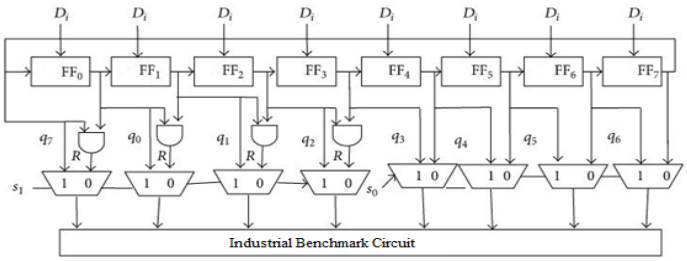

Figure 6: Modified LFSR

4.3.2. Synthesis Report

The table below shows the synthesis report of modified LFSR when used in top module to extract various parameters. The Power consumption during testing, total power, Dynamic power are given in mW and Static power is given in nW, Area is given in number of cells and the total number of gates used.

Table 5: Synthesis of modified LFSR

Parameters	Total Power (mW)	Dynamic Power(mW)	Leakage Power(nW)	Area (cells)	Gates
Modified LFSR	0.13	0.12	0.19	4231	463

4.3.3. Performance Analysis and Results

The different TPGs are implemented using the Cadence EDA Tool using 180nm technology and the test patterns are exported to the MATLAB 7.10 R2010a tool to find out the number of transitions. Simulation and Synthesis has been carried out using the Cadence Tool.
The table below shows the various design trade-offs among the three implementations of LFSRs.
The four Evaluation metrics used are:

1. Total Power
2. Dynamic Power
3. Switching Power
4. Area
5. Gates

Type LFSR → / Parameters ↓	Standard	Bipartite	FSM based	Modified
Total Power (mW)	0.11	0.10	0.13	0.13
Dynamic Power(mW)	0.11	0.10	0.13	0.13
Leakage Power(nW)	0.28	0.23	0.18	0.18
Area (cells)	5980	6534	4370	4231
Gates	587	589	487	463
% of Power Consumption	----	9.2 %	15 %	15 %
% Area overhead	----	---	26 %	29.2 %

Table 6: Tradeoffs among the LFSRs

As table 6 shows the lowest power dissipation is of FSM based LFSR with 0.13 mw of power, though it takes more number of gates with respect to Standard LFSR, here we have focused mainly on reducing the power and hence we have achieved it. As we can see the number of cells obtained FSM based Modified LFSR is optimal.

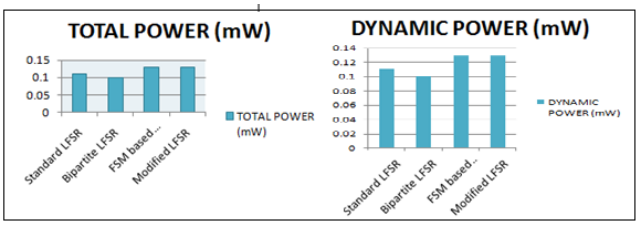

Figure 7. Power analysis

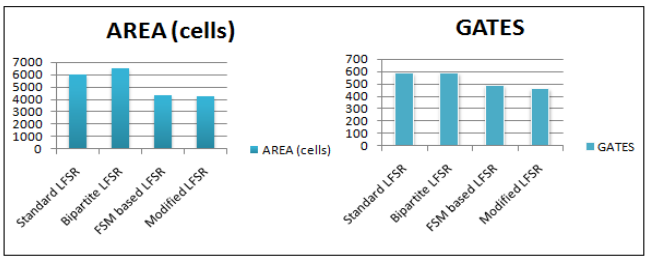

Figure 8. Area overhead analysis

5 .FAULT COVERAGE

The fault coverage for C432benchmark circuits done using Mentor graphics Fast Scan EDA Tool. The top down design flow shown in figure 9. Similarflow can be used to analyze for remaining circuits also. Heredeterministic LFSR is used as ATPG.

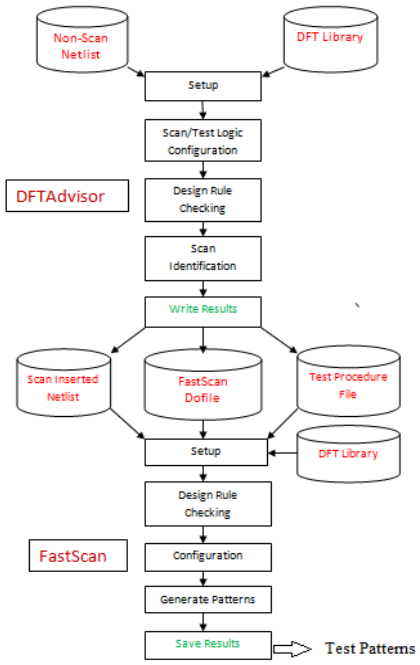

Figure 9. DFT Advisor/Fasts can Design Flow

Table 10.Fault Coverage analysis

Benchmark circuit	Fault Coverage	Test Coverage	ATPG Effectiveness	No of test patterns	Fault Type
C432	98.7%	100%	100%	63	{s_a_0 s_a_1}

6. CONCLUSIONS

This paper presented the design and analysis of FSM based LFSR, Bi-Partite LFSR and Standard LFSR architectures for Logic Built-in Self Test. Among all FSM based LFSR will be having the lowest power consumption while testing the Circuit under Test. Our method for Low Power is based upon reducing the number of transitions. Transitions are reduced in two dimensions: between consecutive patterns (fed to a combinational only circuit) and between consecutive bits (sent to a scan chain in a sequential circuit). Further proposed LFSR modified by freezing control AND gates is independent of circuit under test and flexible to be used in both BIST and scan-based BIST architectures. The modified architecture reduced area compared to other schemes with negligible impact on power and fault coverage. A considerable amount of dynamic power saving (33%) was achieved with the help of this technique. After adding it with leakagepower, we got the net power saving much less compared to other LFSRs. All the calculations are to be done with reference to standard Linear Feedback Shift Register (LFSR).

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